

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1, 3, 4, 11, 13, 14, 31-33, 35 and 36. Also, please cancel claims 2, 5-10, 12, 15-20, 34 and 37-42, which were previously withdrawn and do not depend from an allowable generic claim.

Listing of Claims:

1-20. (Cancelled)

21. (Original) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices; and

a memory hub coupled to the system controller and the memory devices, the memory hub comprising:

a link interface receiving memory requests from the system controller for access to memory cells in at least one of the memory devices, at least some of the memory requests including respective memory hints providing information about the subsequent operation of the memory devices;

a memory device interface coupled to the memory devices and to the link interface, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to dynamically adjust operability of the memory devices responsive to the memory hint.

22. (Original) The memory system of claim 21 wherein the link interface comprises an optical input/output port.

23. (Original) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises signals placing the memory devices in a page mode.

24. (Original) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises a number of pages to remain open.

25. (Original) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises a prefetching hint.

26. (Original) The memory system of claim 21 wherein at least one of the hints comprises a number of cache lines that will be sent from the system controller.

27. (Original) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises a stride indicative of a sequence of addresses from which data are to be fetched.

28. (Original) The memory system of claim 21 wherein at least one of the hints comprises a number of cache lines to skip.

29. (Original) The memory system of claim 21 wherein the memory devices comprise dynamic random access memory devices.

30. (Original) The memory system of claim 21, further comprising a request decoder coupled to the link interface and the memory sequencer, the request decoder being operable to decode the hint.

31-42. (Cancelled)